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| EXAMINER | |
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| VICARY, KEITH E | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/541,275 | PIRES DOS REIS MOREIRA ET AL. | |
| | Examiner | Art Unit | |
| | Keith Vicary | 2183 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *24 December 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-6,8-14 and 16-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-14 and 16-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-6, 8-14, and 16-29 are pending in this office action and presented for examination. Claims 1, 5-6, 8-13, 23-27, and 29 are newly amended and claims 7 and 15 are newly cancelled by amendment filed 12/24/2008.

### *Claim Rejections - 35 USC § 112*

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 8-14, 16-23, 25-27, and 29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claims 8 and 10-12 recite the limitation "Processing system according to claim 7"; however, this is indefinite as claim 7 has been cancelled.

a. Claims 9 and 13-14 are rejected for failing to alleviate the rejection of claim 8 and 12 above.

5. Claims 16-18 recite the limitation "Processing system according to claim 15"; however, this is indefinite as claim 15 has been cancelled.

b. Claims 19-23 are rejected for failing to alleviate the rejection of claim 18 above.

6. Claim 8 recites the limitation "the common control signal" in lines 1-2; however, there is insufficient antecedent basis for this limitation in the claim.

c. Claim 9 is rejected for failing to alleviate the rejection of claim 8 above.

7. Claim 17 recites the limitation "the programmable switches" in line 1; however, there is insufficient antecedent basis for this limitation in the claim.

8. Claim 18 recites the limitation "the programmable switches" in line 1; however, there is insufficient antecedent basis for this limitation in the claim.

d. Claim 19 is rejected for failing to alleviate the rejection of claim 18 above.

9. Claim 25 recites the limitation "the VLIW processors" in line 1; however, there is insufficient antecedent basis for this limitation in the claim.

e. Claims 26-27 are rejected for failing to alleviate the rejection of claim 25 above.

10. Claim 27 recites the limitation "data-path connections going across operation issue slots within the processing elements" in lines 2-3. It is indefinite as to what is being conveyed; for example, connections going "across" operation issue slots does not necessarily mean that the connections are connected to the operation issue slots, and so forth.

11. Claim 29 recites the limitation "combining an intermediate control signal with an operation control signal" in lines 4-5. It is indefinite as to whether this combining is done with, for example, combinational logic, or if a signal of length m is combined with a signal of length n to create a combined signal of length m+n, or so forth.

12. Note that claims 6 and 28 are rejected a second time using an additional art in a manner which more specifically reads on the instant application for the purposes of further prosecution.

***Claim Rejections - 35 USC § 102***

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

14. Claims 1-6, 8, 12-14, 18-22, and 28-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Gove et al. (Gove) (US 5212777).

15. Consider claim 1, Gove discloses a processing system comprising a plurality of processing elements (col. 3, lines 5-6, plurality of processors), the processing elements comprising a controller and computation means (col. 61, lines 28-29 for example, each processing element consists of…the controller and datapath), the plurality of processing elements being dynamically reconfigurable by a cluster control signal as mutually independently operating task units that comprise one processing element or a cluster of two or more processing elements, the processing elements within a cluster being arranged to execute instructions under a common thread of program control (col. 3, lines 5-20, arranging a group of the processors into the SIMD operating mode with circuitry operable on a processor cycle by cycle basis for changing at least some of the processors from the group of processors from operation in the SIMD operating mode to

operation in the MIMD operational mode; also note col. 62, lines 40-52, which discloses that many variations are possible including synchronized MIMD and that any number of the processors could be allocated to any of the modes; the cluster control signal is the execute signal of Figure 2), wherein the cluster control signal is derived from intermediate control signals (Figure 22, the SYNC'D signals in part determine the output of the execute signal) transmitted through a reconfigurable channel infrastructure connected to the processing elements (Figure 22, the wires in which a given signal travels on), wherein the reconfigurable channel infrastructure comprises a control chain with combination elements for each processing element (Figure 22, any given series of NAND gates) and a switch between each pair of neighboring processing elements for locally controllably inhibiting transmission of intermediate control signals to a preceding or a succeeding processing element (Figure 22, any given NAND gate serves as a switch; for example, the left-most NAND gate of Figure 22 prevents an intermediate control signal from transmitting to the second-from-the-left processing element, or one of the group of four vertical NAND gates prevents an intermediate control signal from transmitting to the first-from-the-left processing element from the second-from-the-left processing element. Note that processing element can be read as any logical grouping which includes a controller and computation means, and thus can include, for example, the controller, computation means, and the NAND gate which outputs the execute signal, which enables any of the four vertical NAND gates to be a switch. Alternatively, a switch can be physically located in between the processing elements on either side of the processor to which a switch is associated with).

16. Consider claim 29, Gove discloses of operating a processing system comprising a plurality of processing elements (col. 3, lines 5-6, plurality of processors), the processing elements comprising a controller and computation means (col. 61, lines 28-29 for example, each processing element consists of...the controller and datapath), the method comprising the steps of: combining an intermediate control signal with an operation control signal of a processing element and selectively passing the combined signal to a further processing element (Figure 22, for example, a sync control bit from a given processor is combined with a SYNCD signal from another processing element, the result of which is selectively passed to that given processor's NAND gate which outputs the execute signal; alternatively, the S flag is combined with the OK to sync operation control signal and passed via the bus 40 to other processing elements), deriving a cluster control signal from an operation control signal and two or more intermediate control signals (Figure 22, the execute signal for a processor is derived from sync control bits for that processor, along with SYNCD signals from other processors, as well as other intermediate control signal, such as the signals that directly input into the NAND gate which outputs the execute signal), and dynamically reconfiguring a processing element by the cluster control signal thereby dynamically reconfiguring the plurality of processing elements as mutually independently operating task units, that comprise one processing element or a cluster of two or more processing elements, wherein the processing elements within a cluster execute instructions under a common thread of program control (col. 3, lines 5-20, arranging a group of the

processors into the SIMD operating mode with circuitry operable on a processor cycle by cycle basis for changing at least some of the processors from the group of processors from operation in the SIMD operating mode to operation in the MIMD operational mode; also note col. 62, lines 40-52, which discloses that many variations are possible including synchronized MIMD and that any number of the processors could be allocated to any of the modes; the cluster control signal is the execute signal of Figure 2).

17. Consider claim 2, Gove discloses that processing elements organized in a task unit share at least one common control signal for controlling instruction execution (Figure 22, the SYNC'D signals for example, which are distributed to elements in each task unit which control instruction execution; or the executed signal which each processing unit has when the limitation is interpreted in the same way as the instant specification. Additionally, Figure 4 when an SIMD mode is specified and each processing element fetches from the same instruction memory).

18. Consider claim 3, Gove discloses of conditional branch instructions in, for example, col. 50, lines 49-60. The overall invention of Gove supports the execution of conditional branches in either the SIMD or the synchronized MIMD mode; therefore, the signal which enable or carry out those modes as disclosed above control the conditional jump.

19. Consider claim 4, Gove discloses of conditional branch instructions in, for example, col. 50, lines 49-60. The overall invention of Gove supports the execution of conditional branches in either the SIMD or the synchronized MIMD mode; therefore, the signal which enable or carry out those modes as disclosed above control the conditional jump.

20. Consider claim 5, Gove discloses that the processing elements are connected to each other via data-path connections (Figure 22, the connecting wires).

21. Consider claim 6, Gove discloses the data-path connections (DPC) are limited to neighbour-to-neighbour connections (Figure 22, each processing element can be considered a neighbour in that they are near each other; alternatively, each processing element is a neighbor in that a syncd signal can go straight from one processing element to another via the upper four wires of Figure 22).

22. Consider claim 8, Gove discloses he common control signal is derived by combining the intermediate control signals through a combination element, associated with each processing element (Figure 22, wherein the common control signal is the execution signal and is derived from the various other lines entering in the NAND gates from the processor elements).

23. Consider claim 12, Gove discloses the reconfigurable channel infrastructure comprises mutually transverse chains (Figure 22, for example, chains 40 and the lines vertically connected to that chain; or the horizontal chain emanating from the NAND gate which is inputted the OK TO SYNC signal and the vertically connected lines which lead into the other group of NAND gates).

24. Consider claim 13, Gove discloses the combination elements are arranged in chains having a first orientation and chains having a second orientation (Figure 22, any given series of NAND gates has a respective orientation), and wherein the intermediate control signals transmitted through the chains having the first orientation are forwarded to the combination elements in chains having the second orientation (Figure 22, wherein the first orientation is horizontal from the OK TO SYNC NAND gate and the second orientation is vertical containing the other group of NAND gates, or the first orientation is vertical from the OK TO SYNC NAND gate and the second orientation is horizontal to the other set of four NAND gates; alternatively, the results of the 4 parallel NAND gates are forwarded to another NAND gate that is perpendicular to the aforementioned results).

25. Consider claim 14, Gove discloses the intermediate control signals transmitted through the chains having the second orientation are forwarded to the combination elements in the chains having the first orientation (Figure 22, for example, where the vertically oriented NAND which is inputted the OK TO SYNC signal traverses the

SYNCD set of horizontal lines to another set of four vertical NAND gates as well as the execute-outputting NAND gate, in addition, to its own execute-outputting NAND gate and four vertical NAND gates).

26. Consider claim 18, Gove discloses the programmable switches are programmed by signals stored in memory cells (Figure 22, whether or not the NAND gates let through the SYNCd signal is dependent on how it is programmed by the sync control word, which is disclosed in col. 20, line 59, sync registers).

27. Consider claim 19, Gove discloses at least one of the processing elements can write to at least one of the memory cells (col. 22, lines 58-61, sync bits are set by software depending upon the desired synchronization between the various processors).

28. Consider claim 20, Gove discloses a set of memory cells used to program the switches is organized as a data-word in a memory (col. 20, line 59, each sync register with multi-bit contents can be considered a data-word).

29. Consider claim 21, Gove discloses the memory contains multiple data-words, and wherein the programmable switches are programmed by selecting one of these data-words (Figure 22 and col. 20, line 59, different switches are connected to different sync registers).

30. Consider claim 22, Gove discloses one or more of the processing elements can program the programmable switches by dynamically selecting the data-word in memory (col. 22, lines 58-61, sync bits are set by software depending upon the desired synchronization between the various processors).

31. Consider claim 28, Gove discloses the processing elements are arranged in a 2-dimensional grid (Figure 22, each processor element is in effect part of a 2-dimensional grid).

32. Claims 9-11 and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gove as applied to claims 8 and 15 above, and further in view of Belton (Basic Gate and Functions).

33. Consider claim 9, Gove does not explicitly disclose that the combination elements consist of OR-gates; as seen in Figure 22, NAND gates are used.

Although OR gates were very well known to one of ordinary skill in the art at the time of the invention, Belton explicitly discloses of NAND gates (page 3). Moreover, although the notion that, given desired inputs and outputs, many different combinational logic structures could be used to implement those inputs and outputs, Belton also explicitly discloses that a function in sum of products form can be implemented using NAND gates by replacing all AND and OR gates by NAND gates (page 3, bottom).

It would have been obvious to one of ordinary skill in the art at the time of the invention that it would have been a design choice as to, given desired inputs and outputs, which specific combinational logic structure is used to implement the logic function.

34. Consider claim 10, Gove does not explicitly disclose the channel infrastructure comprises programmable sum-terms; as seen in Figure 22, NAND gates are used.

Although OR gates were very well known to one of ordinary skill in the art at the time of the invention, Belton explicitly discloses of NAND gates (page 3). Moreover, although the notion that, given desired inputs and outputs, many different combinational logic structures could be used to implement those inputs and outputs, Belton also explicitly discloses that a function in sum of products form can be implemented using NAND gates by replacing all AND and OR gates by NAND gates (page 3, bottom).

It would have been obvious to one of ordinary skill in the art at the time of the invention that it would have been a design choice as to, given desired inputs and outputs, which specific combinational logic structure is used to implement the logic function.

35. Consider claim 11, Gove does not explicitly disclose the channel infrastructure comprises programmable product-terms; as seen in Figure 22, NAND gates are used.

Although OR gates were very well known to one of ordinary skill in the art at the time of the invention, Belton explicitly discloses of NAND gates (page 3). Moreover,

although the notion that, given desired inputs and outputs, many different combinational logic structures could be used to implement those inputs and outputs, Belton also explicitly discloses that a function in sum of products form can be implemented using NAND gates by replacing all AND and OR gates by NAND gates (page 3, bottom).

It would have been obvious to one of ordinary skill in the art at the time of the invention that it would have been a design choice as to, given desired inputs and outputs, which specific combinational logic structure is used to implement the logic function.

36. Consider claim 16, Gove does not explicitly disclose the combination elements consist of OR-gates; as seen in Figure 22, NAND gates are used.

Although OR gates were very well known to one of ordinary skill in the art at the time of the invention, Belton explicitly discloses of NAND gates (page 3). Moreover, although the notion that, given desired inputs and outputs, many different combinational logic structures could be used to implement those inputs and outputs, Belton also explicitly discloses that a function in sum of products form can be implemented using NAND gates by replacing all AND and OR gates by NAND gates (page 3, bottom).

It would have been obvious to one of ordinary skill in the art at the time of the invention that it would have been a design choice as to, given desired inputs and outputs, which specific combinational logic structure is used to implement the logic function.

37. Consider claim 17, Gove does not explicitly disclose the programmable switches comprise AND-gates; as seen in Figure 22, NAND gates are used.

Although OR gates were very well known to one of ordinary skill in the art at the time of the invention, Belton explicitly discloses of NAND gates (page 3). Moreover, although the notion that, given desired inputs and outputs, many different combinational logic structures could be used to implement those inputs and outputs, Belton also explicitly discloses that a function in sum of products form can be implemented using NAND gates by replacing all AND and OR gates by NAND gates (page 3, bottom).

It would have been obvious to one of ordinary skill in the art at the time of the invention that it would have been a design choice as to, given desired inputs and outputs, which specific combinational logic structure is used to implement the logic function.

38. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gove as applied to claim 18 above.

39. Consider claim 23, Gove discloses of a sync bits which are located in a sync registers, and thus does not disclose that the sync bits are located in a volatile random access memory (RAM). Gove does disclose of data RAM (Figure 4, element 10) in general.

It would have been readily recognized to one of ordinary skill in the art at the time of the invention that it would have been a design choice as to whether to use a register or RAM to hold values due to the tradeoffs involves, such as speed versus cost.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to replace the register of Gove with a RAM in order to result in cost savings.

40. Claims 24-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gove as applied to claim 1 above, and further in view of Pechanek et al. (Pechanek) (US 6151668).

41. Consider claim 24, Gove does not explicitly disclose each single processing element is capable of executing a VLIW instruction.

On the other hand, Pechanek discloses of each single processing element being capable of executing a VLIW instruction (for example, col. 2, lines 43-48, a VLIW is concurrently executed at an identical address across all PEs).

Pechanek's teaching of executing VLIW instructions increases system performance, as a VLIW instruction performs more operations than a single instruction.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Pechanek with the invention of Gove in order to increase system performance.

42. Consider claim 25, Gove or Pechanek discloses the VLIW processors comprise an internal interconnect network (Figure 22; alternative, it is inherent that inside each processor element there exists an interconnect network, such as from the registers to an ALU and so forth).

43. Consider claim 26, Gove or Pechanek discloses the interconnect network consists of point-to-point connections (Figure 22, it is inherent a processor contains point-to-point connections, or see Gove, Figures 30-33, or the connection between sync control bit 0 and a NAND gate, and so forth, or Pechenak, Figure 5).

44. Consider claim 27, Pechanek discloses the internal interconnect network comprises data-path connections going across operation issue slots within the processing elements (Figure 5, the lines emanating from IR1 to each issue slot and execution unit, for example).

**Second rejection of claims 6 and 28**

45. Claims 6 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gove as applied to claim 1 and 5 above, and further in view of Parcerisa et al. (Efficient Interconnects for Clustered Microarchitectures).

46. Consider claim 6, Gove does not explicitly disclose that the data-path connections are limited to neighbour-to-neighbour connections.

On the other hand, Parcerisa does disclose of a 2-dimensional mesh grid with inter-processor connections made to nearest-neighbor processors only (section 3.5, last pararagraph, mesh).

A 2-dimensional mesh grid is desirable because delays are shorter, due to requiring shorter wires and having smaller parasitic capacitance, network cost is lower, and it is more scalable (Parcerisa, section 3.5, last paragraph).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Parcerisa with the invention of Gove because delays are shorter, due to requiring shorter wires and having smaller parasitic capacitance, network cost is lower, and it is more scalable.

47. Consider claim 28, Gove does not explicitly disclose the processing elements are arranged in a 2-dimensional grid.

On the other hand, Parcerisa does disclose of a 2-dimensional mesh grid with inter-processor connections made to nearest-neighbor processors only (section 3.5, last parargraph, mesh).

A 2-dimensional mesh grid is desirable because delays are shorter, due to requiring shorter wires and having smaller parasitic capacitance, network cost is lower, and it is more scalable (Parcerisa, section 3.5, last paragraph).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Parcerisa with the invention of Gove because delays are shorter, due to requiring shorter wires and having smaller parasitic capacitance, network cost is lower, and it is more scalable. It would have been readily recognized to one of ordinary skill in the art at the time of the invention that the invention of Gove is adaptable to account for the teachings of Parcerisa.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Parcerisa with the invention of Gove in order to map well to planar integrated circuits and maintain link communication at full clock rates.

***Response to Arguments***

48. Examiner acknowledges the general differences between the instant invention and the Gove reference as discussed on pages 8-10; however, the claims as written can still be read broadly such that Gove teaches the claims.

49. Applicant argues on page 10 that Gove does not disclose a "control chain." However, the limitation a "control chain" can be read broadly as done in the rejection above; for example, many elements or logical groups of elements can be considered to be a "chain", and all connections in Figure 22 are directed to controlling the processor. Applicant argues that the NAND gates associated with particular ones of the processing elements cannot inhibit transmission of the synch control signals on synchronization lines 40 to neighboring processing elements. However, this limitation can be met in a variety of ways as explained in the rejection above. For example, the leftmost NAND gate of Figure 22 may inhibit transmission of a certain synch control signal on lines 40 to neighboring processing elements.

50. Applicant argues on page 10 that Applicant's control chain is the antithesis of Gove's universal control bus architecture. However, the limitation "control chain" can nevertheless be broadly interpreted to be an aspect of Gove's architecture.

51. Applicant argues on page 11 that Gove does not include switches inserted between, and controlling passage of intermediate cluster control signals between neighboring processing elements. However, as described in the rejection, Gove does disclose of switches which meet the necessary claimed limitations.

52. Applicant argues on page 11 that claim 29 is distinguishable over Gove in part due to the combining and deriving steps; however, as explained in the rejection, Gove does teach these claimed limitations as well.

53. Applicant argues on pages 11-12 that claim 2 is distinguishable from Gove because SYNCD signals are not control signals to control instruction execution, but instead synchronize processors engaged in a same task. However, synchronizing processors engaged in a same task is one way of controlling instruction execution. Applicant argues that each processing unit receives a separate SYNCD signal. However, each processing unit receives same SYNCD signals; for example, in Figure 22, the output of the leftmost NAND gate is output to each processing element via PP #3 of lines 40. Additionally, the signals outputted from the instruction memory that each

processor element inputs during SIMD mode can also be considered a common control signal in that the instruction controls the execution of the processor.

54. Applicant argues on page 12 that Gove does not disclose that data-path connections are limited to neighbor-to-neighbor connections, because every processor is connected to every other processor. However, each of these processors can be considered to be neighbors with each other as they are all on the same bus. Applicant notes item 54 of the Office action which rejects the claim in an alternate matter; however, a further rejection of a claim in order to further prosecution is not itself evidence that a first rejection is improper.

55. Applicant argues on page 12 the rejection of claim 7 and notes that the element has been incorporated into claim 1; however, a common control signal or the concept that all processing elements output or receive the same execution signal does not appear to be in claim 1.

56. Applicant argues on page 12 that Gove does not disclose of mutually transverse chains, and states that, as defined by Applicants' specification and drawings, "transverse chains" correspond to the vertical and horizontal control chains that, aside from the path orientation, and otherwise equivalent. However, there does not appear to be an explicit definition of "transverse chains" such that claim interpretation must necessarily consider the transverse chains to be other equivalent. In addition, there

does not appear to be an explicit definition that necessitates that the transverse chains correspond to the previously claimed "control chains". Examiner recommends that these concepts be explicitly added to the claims.

57. Applicant argues on pages 12-13 that Gove's NAND gates are not located between pairs of processing elements, but are instead located within each processing element. It is first noted that the limitation "processing element" can be broadly interpreted to include, or exclude, NAND gates, as long as the overall logic which is considered the processing element meets the claimed limitations, e.g. comprises a controller and computation means, is dynamically reconfigurable, and so forth. Alternatively, a switch can be physically located in between the processing elements on either side of the processor to which a switch is associated with.

58. Applicant argues the rejection of claim 24 given the amendment to claim 24. In response, examiner has brought in additional art to teach the newly amended limitations.

59. Applicant argues that the processing elements are not arranged in a 2-dimensional grid. However, regardless of if the processors are connected via a one-dimensional bus structure, the processors themselves are located in a 2-dimensional plane/grid.

***Conclusion***

60. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

f. Barry et al. (US 6167501) discloses of processing element switch connection control for synchronous MIMD mode operations.

g. De Oliveira Kastrup Pereira (US 20060212678) discloses of a reconfigurable processor array exploiting both ILP and TLP.

h. Kravec et al. (US 20050154858) discloses of a chain of control logic for a cascaded processing unit system in Figures 12 and 13.

61. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

62. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Keith Vicary whose telephone number is (571)270-1314. The examiner can normally be reached on Monday - Thursday, 6:15 a.m. - 5:45 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eddie P Chan/
Supervisory Patent Examiner, Art Unit 2183

/Keith Vicary/
Examiner, Art Unit 2183